

WHAT IS CLAIMED IS:

1 1. An interface logic circuit for coupling a domain output of a first logic circuit
2 domain to a domain input of a second logic circuit domain comprising:

3 a first cut-circuit powered by first and second voltage potentials and having a
4 first input coupled to the domain output, and a first output coupled to the domain
5 input, wherein the first voltage potential is coupled to the first cut-circuit in response
6 to a first logic state of a first control signal and decoupled from the first cut-circuit in
7 response to a second logic state of the first control signal; and

8 a latch circuit having a latch input coupled to the first input, and a latch output
9 coupled to the first output, wherein the latch circuit latches logic states at the domain
10 input when the first voltage potential is decoupled from the first cut-inverter.

1 2. The interface logic circuit of claim 1, wherein the latch circuit is powered by
2 the second voltage potential and a third voltage potential, and the third potential is
3 coupled to the latch circuit in response to the second logic state of the first control
4 signal and decoupled from the latch circuit in response to the first logic state of the
5 first control signal.

1 3. The interface logic circuit of claim 2, wherein the second voltage potential is
2 coupled to the first cut-circuit in response to the second logic state of a second control
3 signal and decoupled from the first cut-circuit in response to the first logic state of the
4 second control signal.

1 4. The interface logic circuit of claim 3, wherein the second voltage potential is
2 coupled to the latch circuit in response to the first logic state of the second control
3 signal and decoupled from the latch circuit in response to the second logic state of the
4 second control signal.

1 5. The interface circuit of claim 1, wherein the first cut-circuit comprises:
2 an inverter stage having an inverter input coupled as the input of the first
3 cut_inverter, an inverter output coupled as the output of the first cut_inverter, a first
4 power supply node, and a second power supply node coupled to the second voltage
5 potential; and

6 a first electronic switch coupling the first voltage potential to the first power
7 supply node in response to the first logic state of the first control signal and
8 decoupling the first voltage potential from the first power supply node in response to
9 the second logic state of the first control signal.

1 6. The interface circuit of claim 5, wherein the latch circuit comprises:

2 a first inverter having a first inverter input as the latch input and a first
3 inverter output as the latch output; and

4 a second cut-inverter having an input coupled to the latch output, an output
5 coupled to the latch input, wherein the third voltage potential is coupled to the first
6 cut-inverter in response to the second logic state of a first control signal and
7 decoupled from the second cut-inverter in response to the first logic state of the first
8 control signal.

1 7. The interface circuit of claim 6 further comprising a second electronic switch
2 coupling the second voltage potential to the second power supply node in response to
3 the second logic state of a second control signal and decoupling the second voltage
4 potential from the second power supply node in response to the first logic state of the
5 second control signal.

1 8. The interface circuit of claim 5, wherein the inverter stage comprises
2 an N channel field effect transistor (NFET) having a gate coupled to the
3 inverter input, a source coupled to the second power supply node, and a drain coupled
4 to inverter output; and

5 a P channel field effect transistor (PFET) having a gate coupled to the inverter
6 input, a source coupled to the first power supply node, and a drain coupled to the
7 inverter output.

1 9. The interface circuit of claim 5, wherein the first electronic switch is a PFET
2 having a gate coupled to the first control signal, a drain coupled to the first power
3 supply node, and a source coupled to the first voltage potential.

1 10. The interface circuit of claim 7, wherein the second electronic switch is an
2 NFET having a gate coupled to the second control signal, a drain coupled to the
3 second power supply node, and a source coupled to the second voltage potential.

1 11. The interface circuit of claim 6, wherein the second cut-inverter comprises:
2 an inverter stage having an inverter input coupled as the input of the second
3 cut_inverter, an inverter output coupled as the output of the second cut_inverter, a
4 first latch power supply node, and a second latch power supply node coupled to the
5 second voltage potential; and

6 a third electronic switch coupling the third voltage potential to the first latch
7 power supply node in response to the second logic state of the first control signal and
8 decoupling the third voltage potential from the first latch power supply node in
9 response to first logic state of the first control signal.

1 12. The interface circuit of claim 11 further comprising a fourth electronic switch
2 coupling the second voltage potential to the second latch power supply node in

3 response to the first logic state of the second control signal and decoupling the second
4 voltage potential from the second latch power supply node in response to the second
5 logic state of the second control signal.

1 13. The interface circuit of claim 11, wherein the inverter stage comprises:
2 an N channel field effect transistor (NFET) having a gate coupled to the
3 inverter input, a source coupled to the second power supply node, and a drain coupled
4 to inverter output; and
5 a P channel field effect transistor (PFET) having a gate coupled to the inverter
6 input, a source coupled to the first latch power supply node, and a drain coupled to
7 the inverter output.

1 14. The interface circuit of claim 11, wherein the third electronic switch is an
2 PFET having a gate coupled to a logic inversion of the second control signal, a drain
3 coupled to the first latch power supply node, and a source coupled to the third voltage
4 potential .

1 15. The interface circuit of claim 12, wherein the fourth electronic switch is an
2 NFET having a gate coupled to a logic inversion of the first control signal, a drain
3 coupled to the second latch power supply node, and a source coupled to the second
4 voltage potential.

1 16. The interface logic circuit of claim 11, wherein the first logic circuit domain is
2 a cut-domain with power-gated circuitry and the second domain is a non-cut-domain
3 without power-gated circuitry.

1 17. The interface logic circuit of claim 16, wherein a voltage potential is coupled
2 to the power-gated circuitry in the cut-domain in response to the first logic state of the

3 first control signal and decoupled from the power-gated circuitry in response to the
4 second logic state of the first control signal.

1 18. The interface circuit of claim 1, wherein the latch circuit comprises:
2 a first inverter circuit having a first inverter input as the latch input and a first
3 inverter output as the latch output; and
4 a second inverter circuit having an second inverter input coupled to the first
5 inverter output and a second inverter output coupled to the second inverter output.

1 19. The interface circuit of claim 2, wherein the first and third voltage potentials
2 are equal.

1 20. A data processing system comprising:
2 a central processing unit (CPU);
3 a random access memory (RAM);
4 an input output (I/O) interface unit; and
5 a bus for coupling the CPU, RAM and I/O interface unit, the CPU having first
6 and second logic circuit domains and an interface logic circuit for coupling a domain
7 output from the first logic circuit domain to a domain input to the second logic circuit
8 domain, the interface circuit including a first cut-circuit powered by first and second
9 voltage potentials and having a first input coupled to the domain output, and a first
10 output coupled to the domain input, wherein the first voltage potential is coupled to
11 the first cut-circuit in response to a first logic state of a first control signal and
12 decoupled from the first cut-circuit in response to a second logic state of the first
13 control signal, and a latch circuit having a latch input coupled to the first input, and a
14 latch output coupled to the first output, wherein the latch circuit latches logic states at
15 the domain input when the first voltage potential is decoupled from the first cut-
16 inverter.

1 21. The data processing system of claim 20, wherein the latch circuit is powered
2 by the second voltage potential and a third voltage potential, and the third potential is
3 coupled to the latch circuit in response to the second logic state of the first control
4 signal and decoupled from the latch circuit in response to the first logic state of the
5 first control signal.

1 22. The data processing system of claim 21, wherein the second voltage potential
2 is coupled to the first cut-circuit in response to the second logic state of a second
3 control signal and decoupled from the first cut-circuit in response to the first logic
4 state of the second control signal.

1 23. The data processing system of claim 22, wherein the second voltage potential
2 is coupled to the latch circuit in response to the first logic state of the second control
3 signal and decoupled from the latch circuit in response to the second logic state of the
4 second control signal.

1 24. The data processing system of claim 21, wherein the first and third voltage
2 potentials are equal.